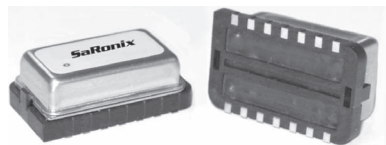


### Technical Data

### STA / STT Series



#### Description

A crystal controlled, low current, low jitter and high frequency oscillator with precise rise and fall times demanded in high performance networking, telecom and processor applications. The tri-state function enables the output to go high impedance. Available in a 14 or an 8 pin DIP compatible, resistance welded, all metal case. Pin 7 (or Pin 4) is grounded to case to reduce EMI. See photo above for new, full size metal package with a true SMD adapter. For this package option select option S in part number builder.

#### Applications & Features

- Fibre Channel
- Gigabit Ethernet
- High performance Processors
- True SMD DIL14 version available
- High Drive HCMOS, AC MOS or TTL capability
- Tri-State output
- Precise Rise/Fall Times
- Reduced EMI circuitry
- Short circuit protected output

Frequency Range:	STT 5V	STA 5V	STA 3.3V
Full Size:	250kHz - 135MHz	125kHz - 135MHz	125kHz - 125MHz
Half Size:	250kHz - 135MHz	500kHz - 135MHz	500kHz - 125MHz
Frequency Stability:	±20, ±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, rated input voltage change, load change, aging*, shock and vibration		
* 1 year @ +40°C			
Temperature Range:			
Operating:	0 to +70°C or -40 to +85°C		
Storage:	-55 to +125°C		
Supply Voltage:			
Recommended Operating:	+5V ±10% or 3.3V ±10% (STA only)		
Supply Current:	50mA typ, 70mA max @ 5V or 30mA typ, 45mA max @ 3.3V		
Output Drive:			
ACMOS / TTL			
Symmetry:	See Part Numbering Guide		
Rise & Fall Times:	See Part Numbering Guide		
Logic 0:	10% VDD or 0.5V max		
Logic 1:	90% VDD or 2.5Vmin		
Load:	50Ω ACMOS, 95Ω ACMOS @ 3.3V, 50mA sink & source @ TTL		
Period Jitter RMS:	8ps max		
Mechanical:			
Shock:	MIL-STD-883, Method 2002, Condition B		
Solderability:	MIL-STD-883, Method 2003		
Terminal Strength:	MIL-STD-202, Method 211, Conditions B2		
Vibration:	MIL-STD-883, Method 2007, Condition A		
Solvent Resistance:	MIL-STD-202, Method 215		
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition A, B or C		
Environmental:			
Gross Leak Test:	MIL-STD-883, Method 1014, Condition C		
Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2		
Thermal Shock:	MIL-STD-883, Method 1011, Conditions A		
Moisture Resistance:	MIL-STD-883, Method 1004		

#### Part Numbering Guide

Series	STA	A	9	9	B	3	-	90.0000	Frequency (MHz)	
STA =	ACMOS compatible, 3.3 or 5V								Supply blank = 5V (STA or STT, 135MHz max) 3 = 3.3V (STA only, 125MHz max)	
STT =	TTL compatible, 5V only									
Symmetry									Stability Tolerance AA = ±20ppm, 80MHz max, 0 to +70°C only A = ±25ppm, 80MHz max, 0 to +70°C only B = ±50ppm C = ±100ppm	
0 =	40/60% max, 0 to +70°C									
A =	45/55% max, 0 to +70°C									
STT to	80 MHz max only									
STA 3.3V to	109.9999 MHz max only								Package Size / Style 0 = Full Size 9 = ½ Size K = Full Size, Gull Wing J = ½ Size, Gull Wing N = ½ Size, Gull Wing, Spanked Leads S = Full Size, True SMD Adapter	
2 =	40/60% max, -40 to +85°C									
STA 3.3V to	109.9999 MHz max only									
Standard* Rise/Fall Times										
1 =	STT 4.0ns max 250kHz to 15 MHz full, to 35 MHz ½ size									
2 =	STT 2.0ns max from 15+ MHz full, 35+ MHz ½ size to 60 MHz									
3 =	STT 1.0ns max from 60+ MHz to 135 MHz									
7 =	STA 5.5ns max, 125kHz to 15 MHz full, 500kHz to 35 MHz ½ size									
8 =	STA 3.5ns max from 15+ MHz full, 35+ MHz ½ size to 60 MHz									
9 =	STA 2ns max from 60+ MHz to 135 MHz(5V), to 125 MHz(3.3V)									

\*R/F times are standard with given frequency ranges, non-standard R/F times available on some models, please contact SaRonix

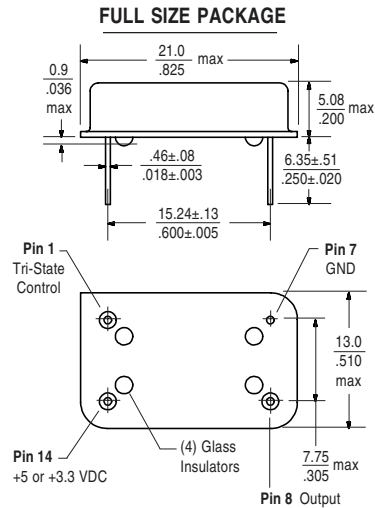
Example PN: STT220C - 60.0000

DS-108 REV K

### Technical Data

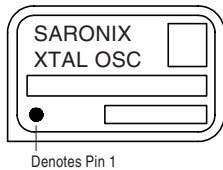
### STA / STT Series

#### Package Details

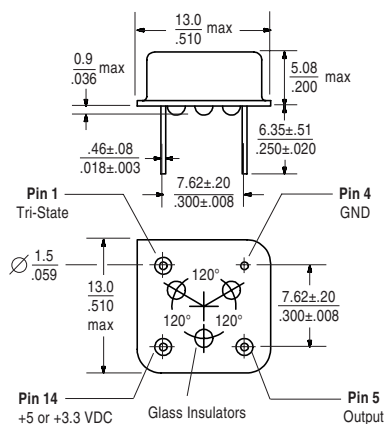


#### Marking Format \*\*

Includes Date Code, Frequency & Part Number

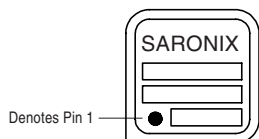


#### HALF SIZE PACKAGE



#### Marking Format \*\*

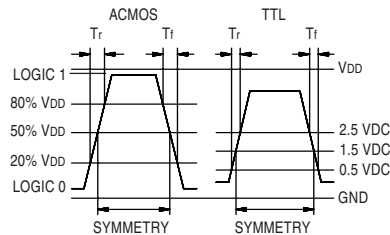
Includes Date Code, Frequency & Part Number



\*\* Exact location of items may vary

Scale: None (Dimensions in mm / inches)

#### Output Waveform



#### Tri-State Logic Table

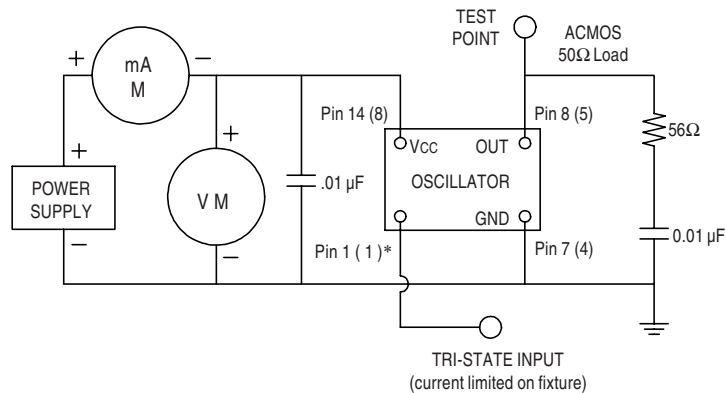
Pin 1 Input	Output Standard Logic
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 1:

Logic 1 = 2.2V min

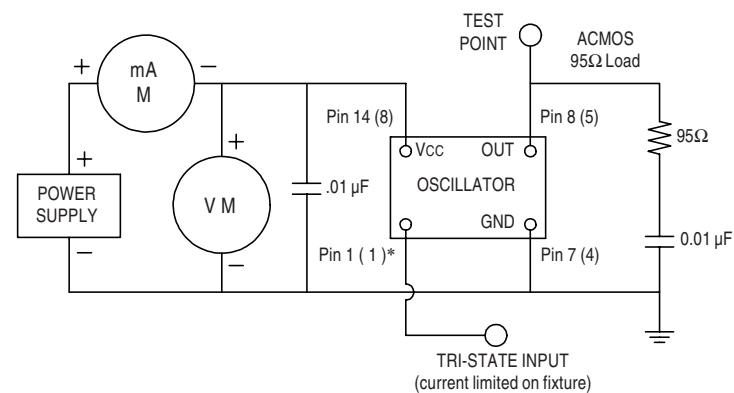
Logic 0 = 0.8V max

#### Test Circuit



\*( ) Indicates pin numbers for half-size package

50Ω AC MOS TEST CIRCUIT (5V operation)



\*( ) Indicates pin numbers for half-size package

95Ω AC MOS TEST CIRCUIT (3.3V operation)

All specifications are subject to change without notice.

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